SPECIFICATION AMENDMENT

1. Please amend paragraph [0061] on page 16 as follows:

[0061] Figs. 11A-11I show different steps in the manufacturing process to create a via for coupling a runner with the backside metal layer as for example shown in FIGs. 1, 3, 5, 7, and 9. Fig. **[[14A]]** **11A** shows the relevant portion of a wafer with substrate 1 and first oxide layer 2 after the dielectric planarization process. At this time a hard mask 110, for example, silicon nitride is used to form mask including at least one window 111 through which a via 130 can be etched. Fig. 11B shows the via 130 after the etching which extends deep into the substrate 1. Optionally, dielectric isolation layers 120 of undoped silicon glass and silicon nitride can be subsequently deposited, in particular within the via to cover the via side walls, as shown in FIG. 11B. However, if contact to a specific area, for example, the source region of a transistor as shown in Figs. 9 and 10 is necessary, no insulation layers will be deposited in the via. Thus, depending on where the via is placed and depending on its function an insulation layer can be used to isolate the via from the surrounding area or no insulation layer is used to couple the surrounding area with the via. Fig. 11C shows another layer 140 on top of layer 120 or a single layer directly deposited after etching of the via which can be obtained through Titanium/Titanium nitride sputter and anneal processes. Fig. **[[14D]]** **11D** **to** **[[14I]]** **11I** show the layers previously deposited as a single layer 190 for a better overview or the single Titanium/Titanium nitride layer (now designated with numeral 1140). In a next step, Tungsten 160 is deposited into the substrate via followed by a Tantalum/Tantalum nitride/Copper seed layer. A copper deposition 170 then follows to fill the substrate via. The surface is then planarized by a chemical mechanical polishing process as shown in Fig. 11D.